An Outer Modem ASIP for Software Defined Radio

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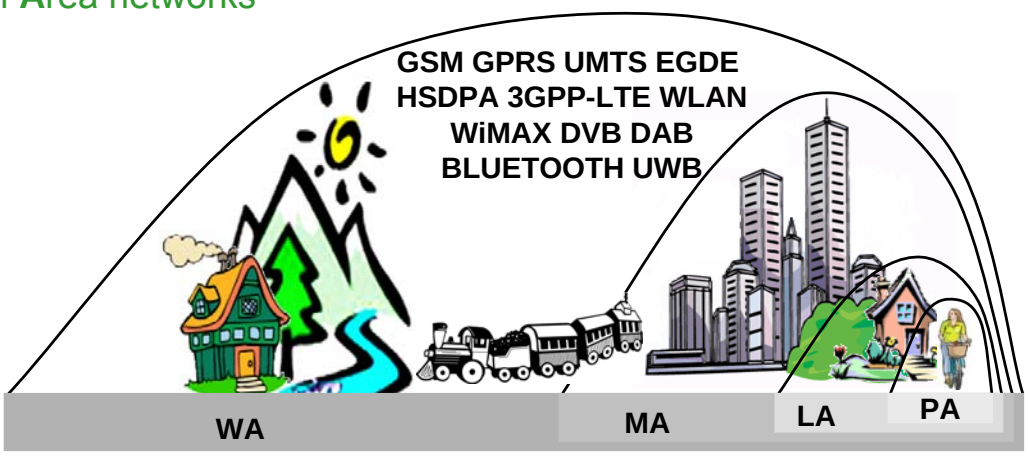
Information Society

Wide **A**rea networks
Metropolitan **A**rea networks
Local **A**rea networks
Personal **A**rea networks

Consumer application
Time-to-Market
NRE-costs Silicon-costs
Low-Power



Wireless Connection any where, any time, any one, any information

Software Defined Radio

Provide flexibility in BB processing but only when valuable!

Inner Receiver: (De)modulation & Channel Estimation

- Techniques in standards different
- Standard signal processing but complex algorithms
- High-level Software flexibility brings large benefit

Programmable (reconfigurable) SIMD/Vector engines

- MUSIC Architecture (Infineon), Sandblaster (Sandbridge), SODA (ARM, Univ. Michigan), SAMIRA (Univ. Dresden)…
- SDR ADRES architecture (IMEC), MONTIUM (Univ. of Twente)

Outer Receiver: (Encoding) Decoding

- Techniques in standards: CC, Turbo-, LDPC Codes
- Complex non standard signal processing arithmetic, non-standard wordwidth
- Data routing and memory architecture are key
- Flexibility required, but limited benefit of high-level software

Standards

Standard	Codes	Rates	States	Blocksizes	Throughput*
GSM	CC	3/4...1/4	16, 64	33...876	...12 kbps
EDGE	CC	6/7,1/3	64	39...870	5...62 kbps
UMTS	CC	1/2,1/3	256	1-504	...32 kbps
	bTC	1/3	8	40-5114	...2 Mbps
HSDPA	bTC	1/2…3/4	8	40-5114	…14.4 Mbps
LTE	bTC	1/3	8	40-5114	…100Mbps
CDMA-2k	CC	1/2...1/6	256	1-744	...28 kbps
	bTC	1/2...1/5	8	378...20736	...2 Mbps
IEEE802.11 a,b,g,n (WLAN)	CC	1/2...3/4	64	1…4095	6...54 Mbps
	CC	2/3	256		
	CC	1/2…5/6	64		…300 Mbps
	LDPC	1/2...5/6	-	...1944	...450 Mbps
DAB	CC	1/4	64	1…4095	1.1 Mbps
IEEE802.16 (WiMax)	CC	1/2...7/8	64	...2040	...54 Mbps
	dbTC	1/2...3/4	8	... 648	...54 Mbps
	LDPC	1/2...5/6	-	...2304	~100Mbps
DVB-T/H	CC	1/4 ...7/8	64	1624	...32 Mbps
DVB-RCT	dbTC	1/2,3/4	16	...648	…31Mbps

* Throughput/Channel

Flexibility/Performance Trade-Off (MPSoC'06)

Weakly programmable decoding engine based on ASIP

- Bottom Up approach to compete with RT-block performance/energy
  - – Start on block architecture level, not on C-Code level
  - – „Just enough flexibility“
- „ASIP unlimited“ (CoWare - ProcessorDesigner)
  - – No constraints on instructions, pipepline, memory structure

Flexibility by programmability

- Instruction level flexibility
- Decoding algorithms

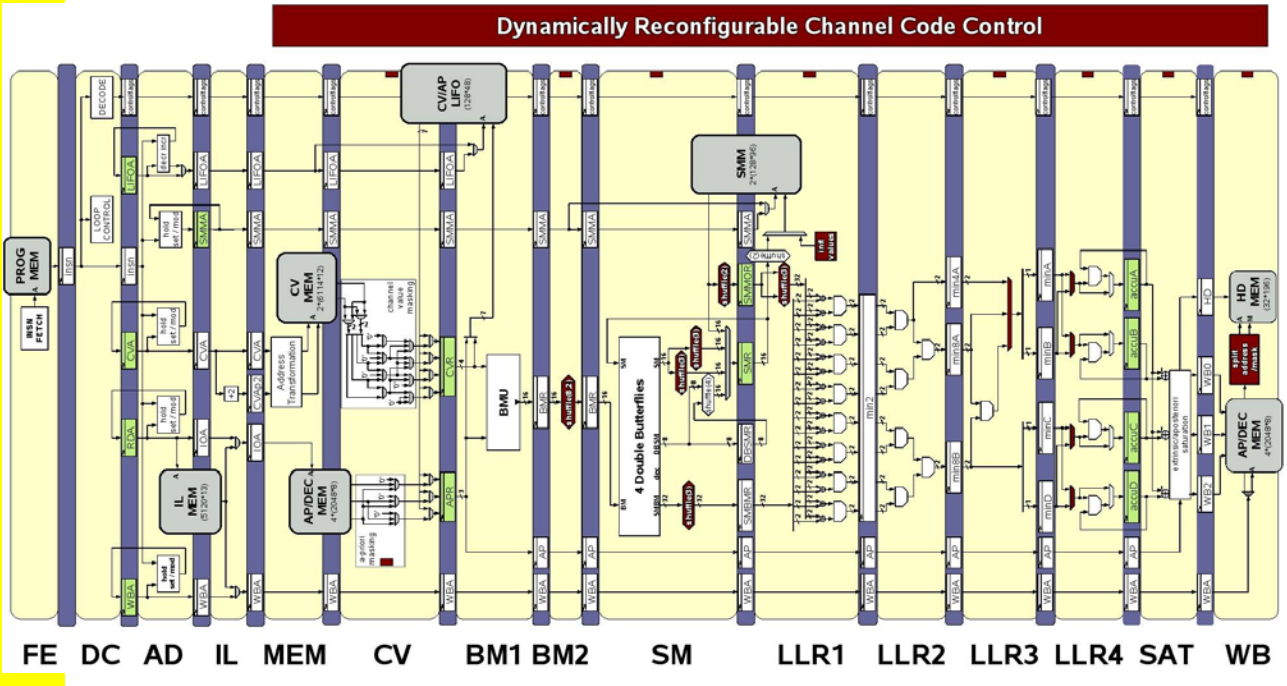
Flexibility by hardware reconfigurability

- Efficient data routing
- Fast context switching and multi context instructions

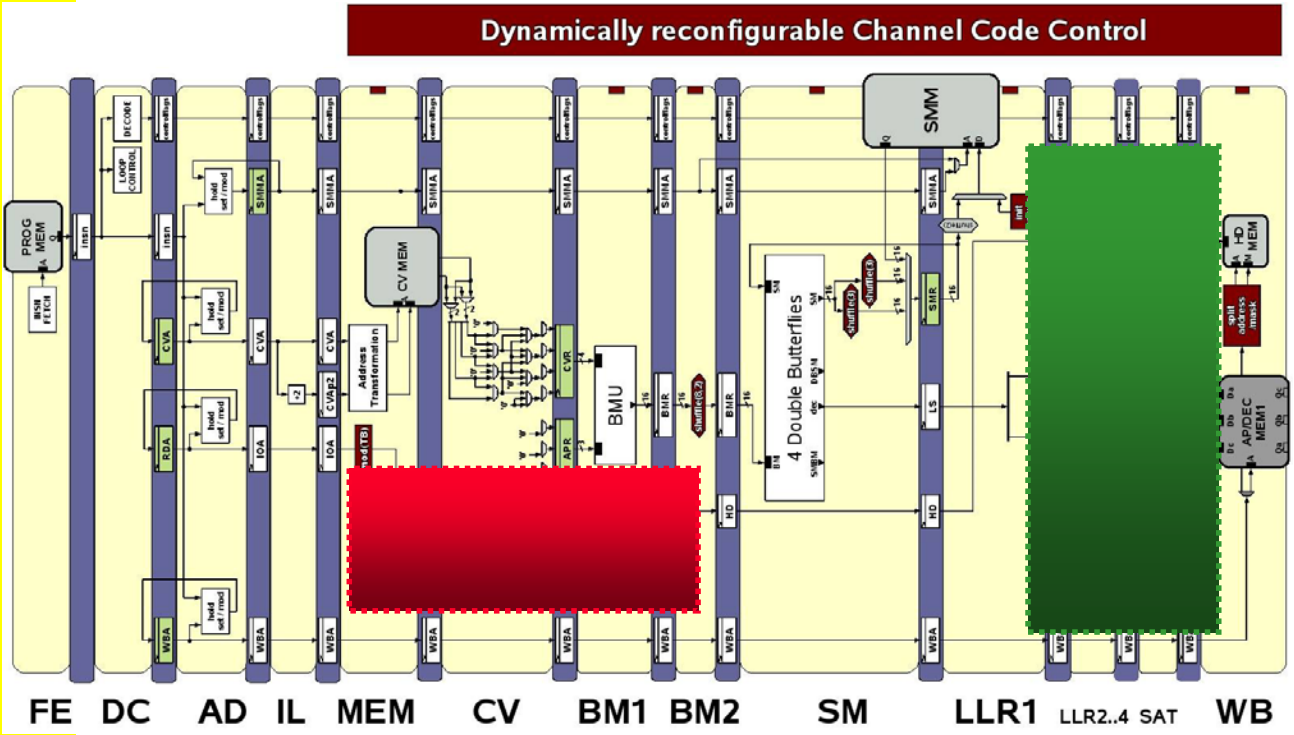
ASIP configured for Turbo Decoding

Supports trellis-based decoding techniques in current standards (FlexiTreP)

- Binary/duo binary Turbo-Code decoding
- Hard/Soft-Output Convolutional decoding



ASIP configured for Viterbi Decoding

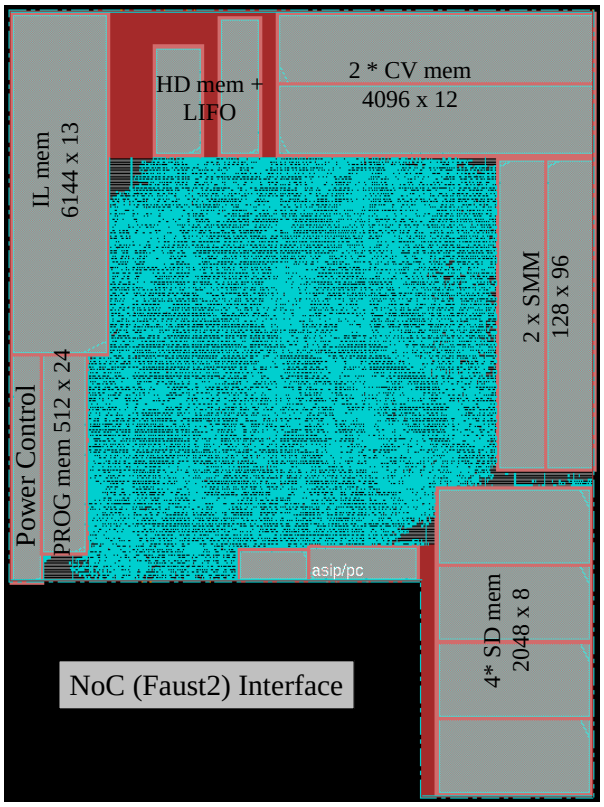


Performance Comparison

	Technology	Frequency	Size
SODA	180nm	400MHz	~1000kGE
ASIP (ENST)	90nm	335MHz	97kGE
FlexiTreP	65nm	400MHz	53kGE

	UMTS bTC		WLAN VA	DVB-RCS dbTC	
	Cycles/bit @5iter	Throughput @5iter	Through-put	Cycles/bit @5iter	Throughput @5iter
SODA	200	2Mbps	24Mbps	?	?
ASIP (ENST)	65	5Mbps	---	37.5	8.6Mbps
FlexiTreP	23.5	17Mbps	44Mbps	11.8	34Mbps

FlexiTreP Layout



- 65nm low power technology
- 41741 standardcells, 15 macros
- Logic density 77,5%
- Die size \wo interface 0,74mm^2
- Frequency 360MHz

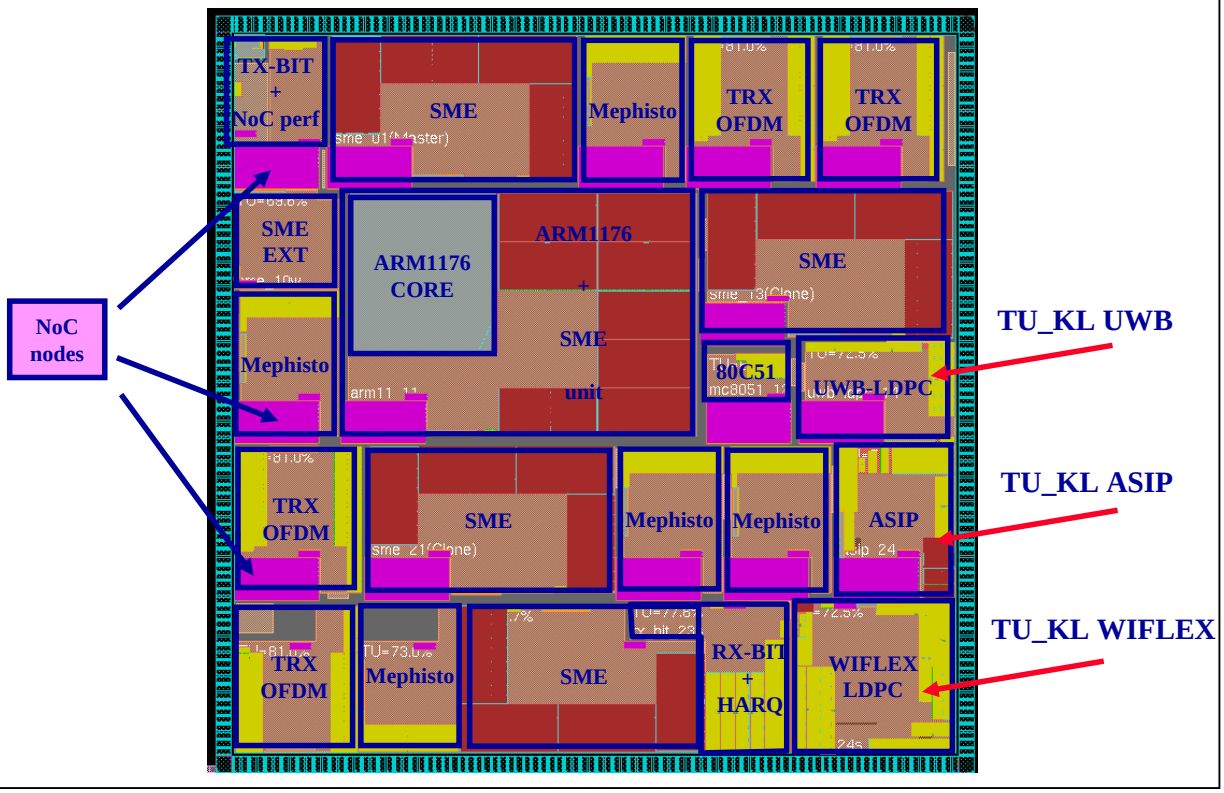
UKL LDPC Decoder Implementations

- LDPC very popular: TC patent issue, performance
- Decoding strongly differs from trellis based decoding
- Standards use permuted identity matrices

LDPC Code	DVB-S2		WiMAX (802.16e) WiFi (802.11n)	U-S LDPC (WiMedia 2.0)
Codeword Size	64800		576-2304	9600
Code Rate	1/4-9/10		1/2-5/6	3/4
Parallelism	90	360	1-32	80
Algorithm	3-Min		MinSum + ESF	
Max. Iterations	50-15		20-10	7
Architecture	1-phase	PN branch	Layered	
Clock frequency	400 MHz		500 MHz	
Area [mm^2] 65nm CMOS				
VNP	0.13	0.22	0	0
CNP	0.33	1.20	0.14	0.24
Network	0.05	0.27	0.01	0.03
Memory	3.36	4.43	0.26	0.37
Overall Area	3.87	6.12	0.43	0.66
Net Throughput	60-708 Mbps	0.23-2.68 Gbps	66-376 Mbps	1.54 Gbps
Latency	270-82 µs	69-21 µs	4.4-5.1 µs	4.7 µs
Max. Efficiency	183 Mbps / mm^2	430 Mbps / mm^2	874 Mbps / mm^2	2.3 Gbps / mm^2

LETI - MAGALI Chip (5400µm * 5400µm)

- NoC (Faust2) based demonstrator for future 4G mobile baseband IPs

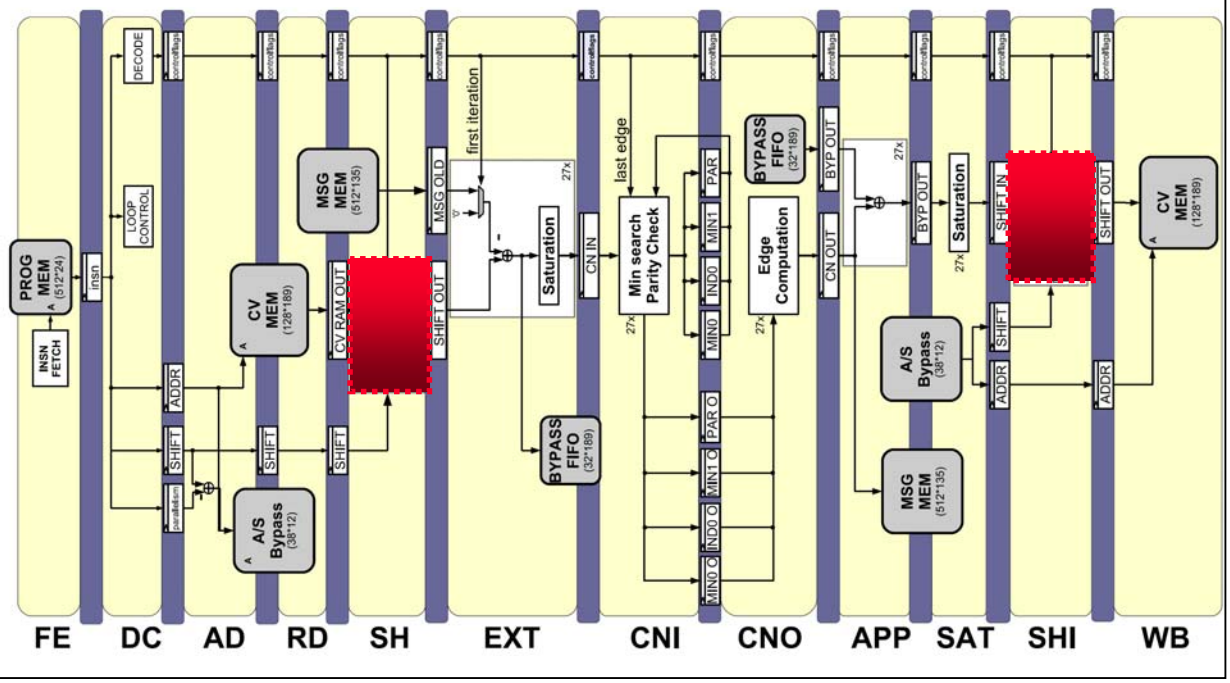


LDPC ASIP approaches

- ASIP Polytecnico di Torino (2006)
  - ASIP as coprocessor for traditional LDPC decoder for matrices based on permuted indentity submatrices
    - processes matrice entries outside of identity submatrices
  - Very low throughput: < 1 Mbps @ 400 MHz @ 20 iterations
- SODA (2007)
  - Inclusion of SIMD LDPC accelerator in SODA pipeline
  - Hardware overhead ~ 5%, Throughput increase ~ 66%
  - Moderate throughput: ~ 15 Mbps @ 400 MHz @ 20 iterations
- IMEC (2008)
  - Highly parallel SIMD architectural study
  - Moderate throughput: ~ 50 Mbps @ 400 MHz @ 20 iterations

ASIP configured for LDPC decoding

- Only reuse of memories and pipeline stages of FlexiTreP
- Two reconfigurable barrel shifters (adaptable to submatrix size)



LDPC Assembler Code

- Supports structured parity-check matrices (WiMAX, WiFi, UWB)
- Example: WiMAX source code (N=576, R=1/2)

```
.text
l.subm 24                    ; reconfigure networks and
                             ; set submatrix size to 24
l.diag 0, s=1,  a=1          ; process submatrix
l.diag 0, s=6,  a=2          ; s determines shift offset
l.diag 0, s=11, a=8          ; a determines address
l.diag 0, s=4,  a=9
l.diag 0, s=23, a=12
l.diag 1, s=0,  a=13         ; last edge of check node

l.diag 0, s=18, a=1          ; new check node begins
l.diag 0, s=19, a=5
l.diag 0, s=5,  a=6
l.diag 0, s=22, a=7
l.diag 0, s=21, a=11
l.diag 0, s=0,  a=13
l.diag 1, s=0,  a=14         ; last edge of check node
...
l.diag 0, s=23, a=12
l.diag 1, s=0,  a=23         ; last edge of check node

l.pchk it=10                 ; perform parity check
nop
PD                           ; power down
```

Synthesis (!) Results

- LDPC Throughput: 27.7 – 257 Mbit/s @ 400 MHz @10-20 iterations

	Standard cells (65nm)		FPGA (Xilinx xc4vlx80-12)	
Functionality	**Area [µm²]**	**Frequency [MHz]**	**Slices**	**Frequency [MHz]**
FlexiTreP (CC/TC)	109320	400	7012	109
LDPC ASIP	113099	425	8076	132
FlexiChaP (CC/TC/LDPC)	232346	400	14495	109

- FlexiTreP 0.11 mm² logic + **0.31mm² memory** = 0.42mm²
- LDPC ASIP 0.11 mm² logic + **0.20mm² memory** = 0.31mm²
- FlexiChaP 0.23 mm² logic + **0.39mm² memory** = 0.62mm²
- LDPC IP Core: 0.11 mm² logic + **0.20mm² memory** = 0.31mm²

Same size but much shorter development time for ASIP!

Conclusion

- Outer Modem in SDR
  - Weakly programmable IP Core
- Weakly programmable IP Core based on
  - „Unlimited“ ASIP approach
  - Application specific data pipelines
  - Distributed data memories
- Efficient memory sharing is key
- Flexibility in several dimensions
  - Design time configurability
  - Low level software programmability
  - Reconfigurability at run-time
- High Throughput
  - Multiprocessor solution

For more information please visit

www.eit.uni-kl.de/wehn